LISTING OF THE CLAIMS

Pursuant to 37 C.F.R. §1.121, provided below is a listing of the claims of the present patent application.

1. (Original) A general purpose performance counter ("GPPC") connected to a bus carrying debug data, the GPPC comprising:

an AND/OR circuit connected to receive the debug data;

a counter circuit connected to receive from the AND/OR circuit an increment signal that, when activated, causes the counter circuit to increment a current count value; and

a compare circuit for activating a match/threshold signal to the AND/OR circuit responsive to a selected block of the debug data having a designated relationship to a compare value,

wherein the AND/OR circuit activates the increment signal responsive to one or more selected bits of an events signal being set.

2. (Original) The GPPC of claim 1 wherein the compare circuit comprises a match circuit for activating the match/threshold signal to the AND/OR circuit when the compare circuit is in match mode and the selected debug data block is equal to the compare value.

3. (Original) The GPPC of claim 1 wherein the compare circuit comprises a threshold circuit for activating the match/threshold signal to the AND/OR circuit when the compare circuit is in threshold mode and the selected debug data block is greater than or equal to the compare value.

4. (Original) The GPPC of claim 1 further comprising a select circuit connected to receive the debug data, the select circuit outputting to the compare circuit a selected block of the debug data identified by a value of a select control signal input thereto.

5. (Original) The GPPC of claim 4 further comprising a zero circuit connected to receive a portion of the selected debug data block from the select circuit, the zero circuit for zeroing out a selected number of most significant bits ("MSBs") of the portion of the selected debug data block input thereto.

6. (Original) The GPPC of claim 5 wherein the zeroed-out portion of the selected debug data block is input to the counter circuit and to the compare circuit.

7. (Original) The GPPC of claim 1 wherein, when the AND/OR circuit is operating in AND mode, the AND/OR circuit activates the increment signal when all of the selected bits of the events signal are set.

8. (Original) The GPPC of claim 1 wherein when the AND/OR circuit is operating in OR mode, the AND/OR circuit activates the increment signal when at least one of the selected bits of the events signal is set.

9. (Original) The GPPC of claim 1 wherein the selected bits of the events signal are selected using a composite mask.

10. (Original) The GPPC of claim 9 wherein the events signal comprises the debug data, the match/threshold signal, and a logic one and wherein the composite mask signal comprises a debug data mask, a threshold/match mask, and an accumulate bit.

11. (Original) The GPPC of claim 1 wherein the debug data comprises 80 bits.

12. (Original) The GPPC of claim 1 wherein the selected block comprises 16 bits and the debug data comprises eight 10-bit-block-aligned blocks.

13. (Original) The GPPC of claim 1 wherein the selected block comprises eight bits.

14. (Original) The GPPC of claim 1 wherein the counter circuit comprises a 48-bit counter.

15. (Original) The GPPC of claim 1 wherein, when the counter circuit is enabled, the counter circuit performs an operation selected from a group consisting of: holding a current count value, incrementing a current count value by one, adding a specified value to the current count value, clearing the current count value, and setting the count value to a specified value.

16. (Original) A general purpose performance counter ("GPPC") connected to a bus carrying debug data, the GPPC comprising:

an AND/OR circuit connected to receive the debug data;

a counter circuit connected to receive from the AND/OR circuit an increment signal that, when activated while the counter circuit is enabled, causes the counter circuit to increment a count value; and

a compare circuit for activating a match/threshold signal to the AND/OR circuit responsive to a selected block of the debug data having a designated relationship to a compare value,

wherein when the AND/OR circuit is in AND mode, the AND/OR circuit activates the increment signal if all of one or more selected bits of an events signal are set and when the AND/OR circuit is in OR mode, the AND/OR circuit activates the increment signal if at least one of the selected bits of the events signal is set.

17. (Original) The GPPC of claim 16 wherein the compare circuit activates the match/threshold signal to the AND/OR circuit when the compare circuit is in match mode and the selected debug data block is equal to the compare value and activates the match/threshold signal to the AND/OR circuit when the compare circuit is in threshold mode and the selected debug data block is greater than or equal to the compare value.

18. (Original) The GPPC of claim 16 further comprising a select circuit connected to receive the debug data and output to the compare circuit a selected block of the debug data identified by a value of a select control signal input thereto.

19. (Original) The GPPC of claim 18 further comprising a zero circuit connected to receive a portion of the selected debug data block from the select circuit, the zero circuit for zeroing out a selected number of most significant bits ("MSBs") of the portion of the selected debug data block input thereto and providing the zeroed-out portion of the selected debug data block to the counter circuit and to the compare circuit.

20. (Original) The GPPC of claim 16 wherein the events signal comprises the debug data, the match/threshold signal, and a logic one.

21. (Original) The GPPC of claim 1 wherein the selected bits of the events signal are selected using a composite mask and wherein the composite mask signal comprises a debug data mask, a threshold/match mask, and an accumulate bit.

22. (Original) The GPPC of claim 16 wherein the debug data comprises 80 bits.

23. (Original) The GPPC of claim 16 wherein the selected block comprises 16 bits and the debug data comprises eight 10-bit-block-aligned blocks.

24. (Original) The GPPC of claim 16 wherein the selected block comprises eight bits.

25. (Original) The GPPC of claim 16 wherein the count value is a 48-bit value.

counter circuit is enabled, the counter circuit performs an operation selected from a group consisting of: holding a current count value, incrementing a current count value by one, adding a specified value to the current count value, clearing the current count value, and setting the count value to a specified value.

26. (Original) The GPPC of claim 16 wherein, when the counter circuit is enabled, the counter circuit performs an operation selected from a group consisting of: holding a current count value, incrementing a current count value by one, adding a specified value to the current count value, clearing the current count value, and setting the count value to a specified value.

27. (Original) A method of implementing a general purpose performance counter ("GPPC") connected to a bus carrying debug data, the method comprising:

providing an AND/OR circuit connected to receive the debug data;

providing a counter circuit connected to receive from the AND/OR circuit an increment signal that, when activated, causes the counter circuit to increment a count; and

providing a compare circuit for activating a match/threshold signal to the AND/OR circuit responsive to a selected block of the debug data having a designated relationship to a compare value; and

activating the increment signal by the AND/OR circuit responsive to one or more selected bits of an events signal being set.

28. (Original) The method of claim 27 further comprising activating the match/threshold signal by the compare circuit to the AND/OR circuit when the compare circuit is in match mode and the selected debug data block is equal to the compare value.

29. (Original) The method of claim 27 further comprising activating the match/threshold signal by the compare circuit to the AND/OR circuit when the compare circuit is in threshold mode and the selected debug data block is greater than or equal to the compare value.

30. (Original) The method of claim 27 further comprising:

providing a select circuit connected to receive the debug data; and

outputting by the select circuit to the match/threshold circuit a selected block of the debug data identified by a value of a select control signal input thereto.

31. (Original) The method of claim 30 further comprising:

providing a zero circuit connected to receive a portion of the selected debug data block from the select circuit; and

the zero circuit zeroing out a selected number of most significant bits ("MSBs") of the portion of the selected debug data block input thereto.

32. (Original) The method of claim 31 further comprising inputting the zeroed-out portion of the selected debug data block to the counter circuit and to the compare circuit.

33. (Original) The method of claim 27 further comprising the AND/OR circuit activating the increment signal when the AND/OR circuit is in AND mode and all of the one or more selected bits of the events signal are set.

34. (Original) The method of claim 27 further comprising the AND/OR circuit activating the increment signal when the AND/OR circuit is in OR mode and the at least one of one or more selected bits of the events signal are set.

35. (Original) The method of claim 27 further comprising selecting one or more bits of the events signal using a composite mask.

36. (Original) The method of claim 27 further comprising:

enabling the counter circuit; and

responsive to the counter circuit being enabled, the counter circuit performing an operation selected from a group consisting of: holding a current count value, incrementing a current count value by one, adding a specified value to the current count value, clearing the current count value, and setting the count value to a specified value.